The SimSoC full simulation system

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The development of embedded systems platforms requires increasingly large amount of software running on complex System On Chips. In order to validate such systems has emerged the concept of "virtual prototyping". A virtual prototyping environment is a suite of software tools that allow for the development of embedded systems and make possible to test them (hardware and software) even though no real hardware has been manufactured. The cornerstone of a virtual prototyping environment is the simulation platform that is necessary to simulate the system under design so that software developers can test the software and hardware developers can investigate design alternatives.

For the embedded software developers, the simulation environment must achieve full system simulation: it must run the exact binary software that will be shipped with the product, including the operating system and the embedded application; and the simulation must be fast enough for interactive testing and fast software verification cycles. Modularity and fast prototyping also have become important aspects of simulation frameworks, for investigating alternative designs with easier re-use and integration of third party IP's. These requirements call for an integrated, modular, full simulation environment where already proven components can be simulated quickly whereas new IP under design can be tested more thoroughly.

A full system simulation at low level of hardware detail (cycle accurate) is much too slow for the purpose of software testing. In order to reach fast simulation speed (above 100 Millions instructions per second) it is necessary to use other techniques, in particular dynamic translation of the application software and simulation of the hardware at a higher level of abstraction than the VHDL level.

The FORMES joint project between France and China is developing a simulation framework geared towards virtual prototyping including full system simulation. The SimSoC simulation framework uses Transaction Level Modeling for modeling hardware components, based on the System/C open standard, with an implementation based on the OSCI open source library. The hardware models are standard SystemC TLM abstractions and the simulator uses the standard SystemC kernel. Therefore, the simulation host can be any commodity commercial off-the-shelf computer and yet provide reasonable simulation performance.

To achieve fast processor simulation, the Simsoc Instruction Set Simulation technology uses a form of dynamic translation, using an intermediate representation and pre-generated code using specialization, a technique already used within virtual machines.

In the full paper, we will explain explains the overall structure of the simulator, the integration between SystemC, TLM and the ISS, describes the dynamic translation technology, and report performance benchmarks. Finally the conclusion will offer perspectives for improving simulation speed.
At the moment of this writing, the software is not yet distributed as open source because it is not considered stable enough to be distributed. We hope this can be achieved for the conference time.